Refine Search

Search Results -

Terms	Documents
request same (unidirectional or (uni adj1 directional)) same bus same arbit$6	139

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, March 15, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	request same (unidirectional or (uni adj1 directional)) same bus same arbit$6	139	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
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IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, March 15, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	request same (unidirectional or (uni adj1 directional)) same bus same arbit$6	139	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(370/462 |710/107 |710/113 |710/305 |710/240 |710/241 |710/316 |710/52 |340/825).ccls.	5921

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
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- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, March 15, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	710/107,113,305,240,241,316,52;340/825;370/462.ccls.	5921	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	request same (unidirectional or (uni adj1 directional)) same bus same arbit$6	139	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L3	32

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, March 15, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	l1 and L3	32	L4
L3	710/107,113,305,240,241,316,52;340/825;370/462.ccls.	5921	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	request same (unidirectional or (uni adj1 directional)) same bus same arbit$6	139	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L4 and buffer and multiplexer	12

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, March 15, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L6	L4 and buffer and multiplexer	12	L6
L5	L4 and buffer	25	L5
L4	l1 and L3	32	L4
L3	710/107,113,305,240,241,316,52;340/825;370/462.ccls.	5921	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	L1	0	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	request same (unidirectional or (uni adj1 directional)) same bus same arbit$6	139	L1

END OF SEARCH HISTORY

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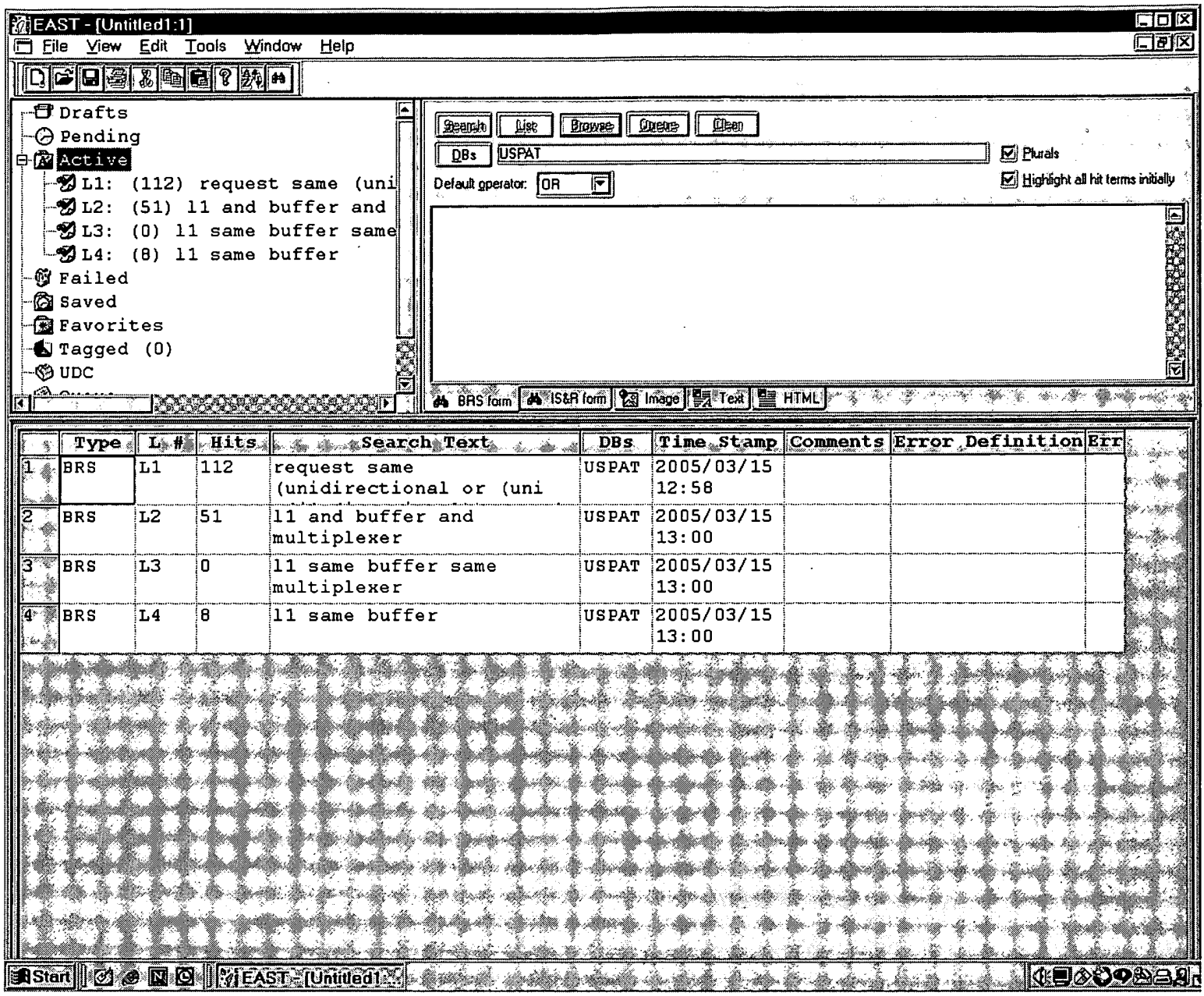
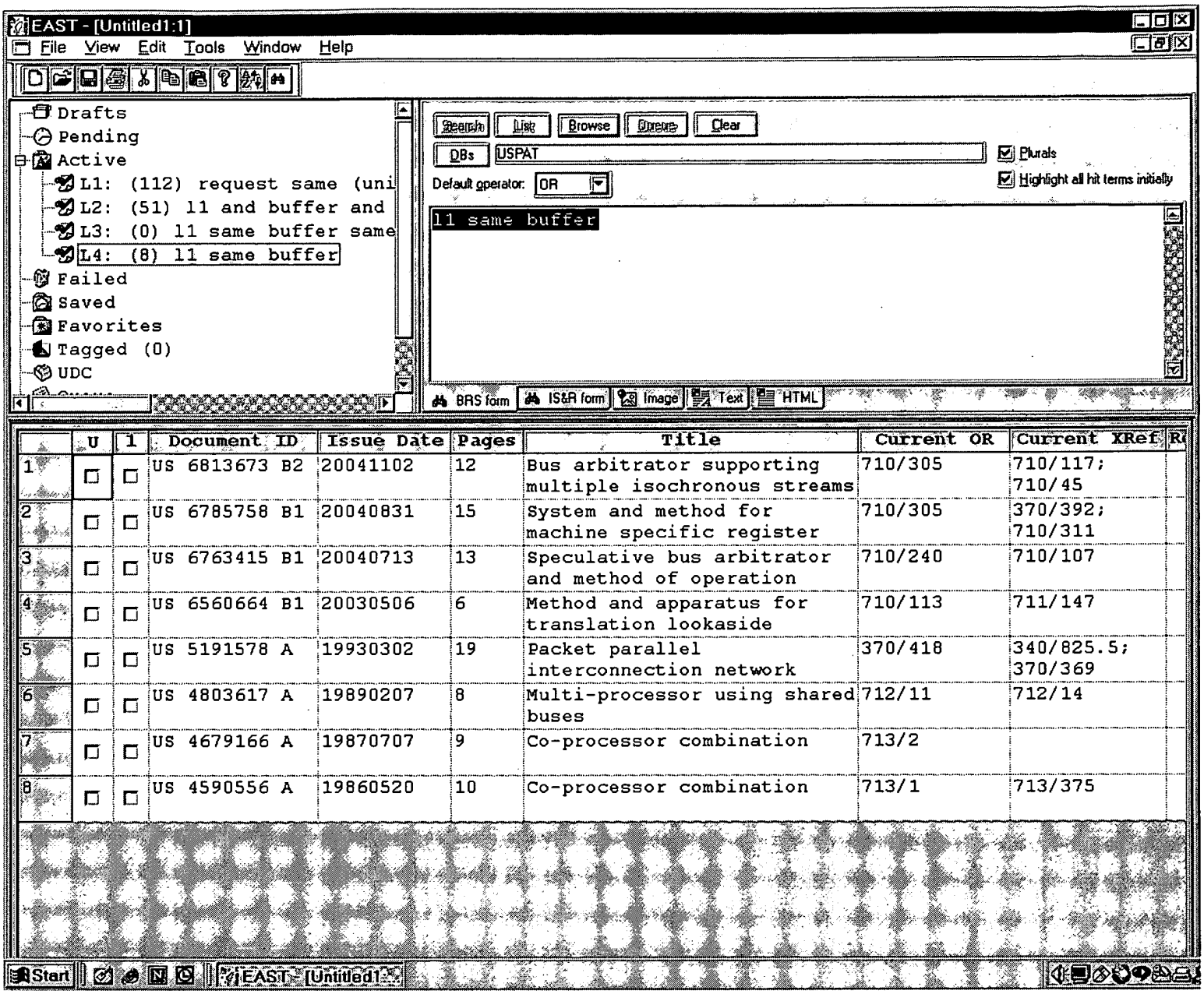

EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (112) request same (uni
L2: (51) l1 and buffer and
L3: (0) l1 same buffer same
L4: (8) l1 same buffer
Failed
Saved
Favorites
Tagged (0)
UDC
Search List Browse Create Clear
DBs USPAT
Plurals
Default operator: OR
Highlight all hit terms initially
BRS form IS&R form Image Text HTML
Type L # Hits Search Text DBs Time Stamp Comments Error Definition Err
1 BRS L1 112 request same (unidirectional or (uni USPAT 2005/03/15 12:58
2 BRS L2 51 l1 and buffer and multiplexer USPAT 2005/03/15 13:00
3 BRS L3 0 l1 same buffer same multiplexer USPAT 2005/03/15 13:00
4 BRS L4 8 l1 same buffer USPAT 2005/03/15 13:00
Start
EAST - [Untitled1



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6813673 B2	20041102	12	Bus arbitrator supporting multiple isochronous streams	710/305	710/117; 710/45	
2	☐	☐	US 6785758 B1	20040831	15	System and method for machine specific register	710/305	370/392; 710/311	
3	☐	☐	US 6763415 B1	20040713	13	Speculative bus arbitrator and method of operation	710/240	710/107	
4	☐	☐	US 6560664 B1	20030506	6	Method and apparatus for translation lookaside	710/113	711/147	
5	☐	☐	US 5191578 A	19930302	19	Packet parallel interconnection network	370/418	340/825.5; 370/369	
6	☐	☐	US 4803617 A	19890207	8	Multi-processor using shared buses	712/11	712/14	
7	☐	☐	US 4679166 A	19870707	9	Co-processor combination	713/2		
8	☐	☐	US 4590556 A	19860520	10	Co-processor combination	713/1	713/375	

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request and bus and arbit* Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A dual round-robin arbiter for split-transaction buses in system-on-c implementations**
Reed, J.; Manjikian, N.;
Electrical and Computer Engineering, 2004. Canadian Conference on , Volume 2 , 2-5 May 2004
Pages:835 - 840 Vol.2

[Abstract] [PDF Full-Text (511 KB)] **IEEE CNF**

---

2 **Decentralized arbiter design for a synchronous hierarchical bus multiprocessor system**
Alam, M.S.; Karim, M.A.;
Aerospace and Electronics Conference, 1992. NAECON 1992., Proceedings of t IEEE 1992 National , 18-22 May 1992
Pages:187 - 192 vol.1

[Abstract] [PDF Full-Text (364 KB)] **IEEE CNF**

---

3 **Impact of bus arbitration on the schedulability of real-time shared-t multiprocessors**
Chang Yeol Choi; Heonshik Shin;
TENCON '94. IEEE Region 10's Ninth Annual International Conference. Theme 'Frontiers of Computer Technology'. Proceedings of 1994 , 22-26 Aug. 1994
Pages:602 - 606 vol.2

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

---

4 **A new arbitration circuit for asynchronous multiple bus multiproces systems**
Mahmud, S.M.; Sheth, D.G.; Alles, S.A.;

h eee e eee g e ch e ch e e e e b b c

Circuits and Systems, 1991., IEEE International Sympoisum on , 11-14 June 1
Pages:1041 - 1044 vol.2

[Abstract] [PDF Full-Text (320 KB)] IEEE CNF

---

5 **Performance model for a prioritized multiple-bus multiprocessor sys**
John, L.K.; Yu-Cheng Liu;
Computers, IEEE Transactions on , Volume: 45 , Issue: 5 , May 1996
Pages:580 - 588

[Abstract] [PDF Full-Text (724 KB)] IEEE JNL

---

6 **A comprehensive performance evaluation of crossbar networks**
Youn, H.Y.; Chen, C.C.-Y.;
Parallel and Distributed Systems, IEEE Transactions on , Volume: 4 , Issue: 5
1993
Pages:481 - 489

[Abstract] [PDF Full-Text (676 KB)] IEEE JNL

---

7 **Evaluation of reservation-arbitrated access schemes for statistical multiplexing of variable-bit-rate video traffic over dual-bus metropoli area networks**
Chan, H.C.B.; Leung, V.C.M.;
Communications, IEE Proceedings- , Volume: 145 , Issue: 3 , June 1998
Pages:159 - 167

[Abstract] [PDF Full-Text (700 KB)] IEE JNL

---

8 **Performance model for a prioritized multiple-bus multiprocessor sys**
Kurian, L.; Yu-Cheng Liu;
Parallel and Distributed Processing, 1994. Proceedings. Sixth IEEE Symposiur
on , 26-29 Oct. 1994
Pages:577 - 584

[Abstract] [PDF Full-Text (488 KB)] IEEE CNF

---

9 **A comprehensive modeling for performance evaluation of regular interconnection network**
Chen, C.C.-Y.; Hee Yong Youn;
Parallel and Distributed Processing, 1990. Proceedings of the Second IEEE
Symposium on , 9-13 Dec. 1990
Pages:768 - 775

[Abstract] [PDF Full-Text (524 KB)] IEEE CNF

---

10 **A fair distributed queue dual bus access method**
Khalil, K.M.; Koblentz, M.E.;
Local Computer Networks, 1989., Proceedings 14th Conference on , 10-12 Oc
1989
Pages:180 - 188

[Abstract] [PDF Full-Text (564 KB)] IEEE CNF

---

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11 **Distributed round-robin and first-come first-serve protocols and th application to multiprocessor bus arbitrary**
Vernon, M.K.; Manber, U.;
Computer Architecture, 1988. Conference Proceedings. 15th Annual Internatic Symposium on , 30 May-2 June 1988
Pages:269 - 277

[Abstract] [PDF Full-Text (908 KB)] **IEEE CNF**

---

12 **Comments on `Design and analysis of arbitration protocols' by F. E Guibaly**
Wilkinson, B.;
Computers, IEEE Transactions on , Volume: 41 , Issue: 3 , March 1992
Pages:348 - 351

[Abstract] [PDF Full-Text (344 KB)] **IEEE JNL**

---

13 **Fast system-level design space exploration for low power configura multimedia systems-on-chip**
Polloni, F.; Mazzoni, L.; Di Matteo, S.;
ASIC/SOC Conference, 2002. 15th Annual IEEE International , 25-28 Sept. 20
Pages:150 - 154

[Abstract] [PDF Full-Text (418 KB)] **IEEE CNF**

---

14 **Fuzzy logic arbiters for multiple-bus multiprocessor systems**
Diab, H.B.;
Systems, Man and Cybernetics, Part C, IEEE Transactions on , Volume: 34 , Is 3 , Aug. 2004
Pages:281 - 292

[Abstract] [PDF Full-Text (480 KB)] **IEEE JNL**

---

15 **A 4K/spl times/8 dynamic RAM with self-refresh**
Reese, E.A.; Spaderna, D.W.; Flannagan, S.T.; Tsang, F.;
Solid-State Circuits, IEEE Journal of , Volume: 16 , Issue: 5 , Oct 1981
Pages:479 - 487

[Abstract] [PDF Full-Text (1136 KB)] **IEEE JNL**

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1 2 Next

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Performance model for a prioritized multiple-bus multiprocessor system

John, L.K. Yu-Cheng Liu
Dept. of Comput. Sci. & Eng., Univ. of South Florida, Tampa, FL, USA;
This paper appears in: **Computers, IEEE Transactions on**

Publication Date: May 1996
On page(s): 580 - 588
Volume: 45 , Issue: 5
ISSN: 0018-9340
Reference Cited: 24
CODEN: ITCOB4
Inspec Accession Number: 5294010

Abstract:
The performance of a shared memory multiprocessor system with a multiple-**bus** interconnection network is studied in this paper. The effect of **bus** and memory contention is modeled using a probabilistic model and a closed form solution for the acceptance probability of each processor is presented. It is assumed that each processor in the system has a distinct priority assigned to it and that **arbitration** is based on priority. Whenever a **request** from a processor is rejected due to **bus** or memory conflicts, the **request** is resubmitted until granted. Based on the model, individual

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processor acceptance probabilities are first estimated, from which the effective memory bandwidth is computed. The accuracy of the analytical model is verified based on simulation results. Results from the model are compared against other approximate models previously reported in literature. It is observed that the inaccuracy of the model measured in terms of error from simulation results is less than that in previously reported studies

Index Terms:

multiprocessing systems performance evaluation shared memory systems acceptance probabilities acceptance probability **arbitration** distinct priority memory bandwidth multiple-**bus** interconnection network performance prioritized multiple-**bus** multiprocessor shared memory multiprocessor system

Documents that cite this document

There are no citing documents available in IEEE Xplore at this time.

Reference list:

1, D.P. Bhandarkar,, "Analysis of Memory Interference in Multiprocessors," *IEEE Trans. Computers,* vol. 24, no. 9, pp. 897-908, Sept. 1975.
[Buy Via Ask*IEEE]

2, L.N. Bhuyan,, "An Analysis of Processor Memory Interconnection Networks," *IEEE Trans. Computers,* vol. 34, no. 3, pp. 279-283, Mar. 1985.
[Buy Via Ask*IEEE]

3, L.N. Bhuyan,, Q. Yang and D.P. Agrawal,, "Performance of Multiprocessor Interconnection Networks," *Computer,* vol. 22, no. 2, pp. 25-37, Feb. 1989.
[Abstract] [PDF Full-Text (928KB)]

4, L.N. Bhuyan and D.P. Agrawal,, "Design and Performance of Generalized Interconnection Networks," *IEEE Trans. Computers,* vol. 32, no. 12, pp. 1,081-1,090, Dec. 1983.
[Buy Via Ask*IEEE]

5, D.Y. Chang,, D.J. Kuck and D.H. Lawrie,, "On the Effective Bandwidth of Parallel Memories," *IEEE Trans. Computers,* vol. 26, no. 5, pp. 480-489, May 1977.
[Buy Via Ask*IEEE]

h eee e eee g e ch ch b c be be be c e eee

6, W.T. Chen and J.P. Shen,, "Performance Analysis of Multiple Bus Interconnection Networks with Hierarchical Requesting Model," *IEEE Trans. Computers,* vol. 40, no. 7, pp. 834-842, July 1991.
[Abstract] [PDF Full-Text (744KB)]

7, C.R. Das and L.N. Bhuyan,, "Bandwidth Availability of Multiple Bus Multiprocessors," *IEEE Trans. Computers,* vol. 34, no. 10, pp. 918-926, Oct. 1985.
[Buy Via Ask*IEEE]

8, T.Y. Feng,, "A Survey of Interconnection Networks," *Computer,* vol. 14, no. 12, pp. 12-27, Dec. 1981.
[Buy Via Ask*IEEE]

9, M.A. Holliday and M.K. Vernon,, "Exact Performance Estimates for Multiprocessor Memory and Bus Interference," *IEEE Trans. Computers,* vol. 36, no. 1, pp. 76-85, Jan. 1987.
[Buy Via Ask*IEEE]

10, K. Hwang and F.A. Briggs,, *Computer Architecture and Parallel Processing.*New York: McGraw Hill, 1984.
[Buy Via Ask*IEEE]

11, L. Kurian,, "Performance Evaluation of Prioritized Multiple-Bus Multiprocessor Systems," MS thesis, Dept of Electrical Eng., Univ. of Texas, El Paso, Dec. 1989.

12, T. Lang,, M. Valero and I. Alegre,, "Bandwidth of Crossbar and Multiple-Bus Connections for Multiprocessors," *IEEE Trans. Computers,* vol. 31, no. 12, pp. 1,227-1,234, Dec. 1982.
[Buy Via Ask*IEEE]

13, Y.C. Liu and C.J. Jou,, "Effective Memory Bandwidth and Processor Blocking Probability in Multiple-Bus Systems," *IEEE Trans. Computers,* vol. 36, no. 6, pp. 761-764, June 1987.
[Buy Via Ask*IEEE]

14, Y.C. Liu and C.C. Wang,, "Analysis of Prioritized Crossbar Multiprocessor Systems," *J. Parallel and Distributed Computing,* vol. 7, pp. 321-334, Oct. 1989.
[Buy Via Ask*IEEE] [CrossRef]

15, S.M. Mahmud,, "Performance of Multilevel Bus Networks for Hierarchical Multiprocessors," *IEEE Trans. Computers,* vol. 43, no. 7, pp. 789-805, July 1994.
[Abstract] [PDF Full-Text (1288KB)]

16, M.A. Marsan,, G. Balbo,, G. Conte and F. Gregoretti,, "Modeling Bus Contention and Memory Interference in a Multiprocessor System," *IEEE Trans. Computers,* vol. 32, no. 1, pp. 60-72, Jan. 1983.
[Buy Via Ask*IEEE]

17, T.N. Mudge,, J.P. Hayes,, G.D. Buzzard and D.C. Winsor,, "Analysis of Multiple-Bus Interconnection Networks," *J. Parallel and Distributed Computing,* vol. 3, pp. 328-343, Mar. 1986.
[Buy Via Ask*IEEE] [CrossRef]

18, T.N. Mudge,, J.P. Hayes,, G.D. Buzzard and D.C. Winsor,, "Analysis of Multiple-Bus Interconnection Networks," *Proc. 1984 Conf. Parallel Processing,* pp. 228-232, Aug. 1984.
[Buy Via Ask*IEEE]

19, T.N. Mudge and H.B. Al-Sadoun,, "A Semi-Markov Model for the Performance of Multiple-Bus Systems," *IEEE Trans. Computers,* vol. 34, no. 10, pp. 934-942, Oct. 1985.
[Buy Via Ask*IEEE]

20, C.V. Ravi,, "On the Bandwidth and Interference in Interleaved Memory Systems," *IEEE Trans. Computers,* vol. 21, no. 8, pp. 899-901, Aug. 1972.
[Buy Via Ask*IEEE]

21, E.C. Russel,, "Building Simulation Models with SIMSCRIPT II.5," CACI Products Company, La Jolla, Calif.

22, D. Towsley,, "Approximate Models of Multiple-Bus Multiprocessor Systems," *IEEE Trans. Computers,* vol. 35, no. 3, pp. 220-228, Mar. 1986.
[Buy Via Ask*IEEE]

23, Q. Yang and S. Zaky,, "Communication Performance in Multiple-Bus Systems," *IEEE Trans. Computers,* vol. 37, no. 7, July 1988.
[Abstract] [PDF Full-Text (528KB)]

24, D.W.L. Yen,, J.H. Patel and E.S. Davidson,, "Memory Interference in Synchronous Multiprocessor Systems," *IEEE Trans. Computers,* vol. 31, no. 11, pp. 1,116-1,121, Nov. 1982.
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☐ 1. Document ID: US 6587905 B1

Using default format because multiple data bases are involved.

L6: Entry 1 of 12 File: USPT Jul 1, 2003

US-PAT-NO: 6587905
DOCUMENT-IDENTIFIER: US 6587905 B1

TITLE: Dynamic data bus allocation

DATE-ISSUED: July 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Correale, Jr.; Anthony	Raleigh	NC		
Hofmann; Richard Gerard	Apex	NC		
LaFauci; Peter Dean	Holly Springs	NC		
Wilkerson; Dennis Charles	Durham	NC		

US-CL-CURRENT: 710/107; 710/110, 710/244

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 2. Document ID: US 6560664 B1

L6: Entry 2 of 12 File: USPT May 6, 2003

US-PAT-NO: 6560664
DOCUMENT-IDENTIFIER: US 6560664 B1

TITLE: Method and apparatus for translation lookaside buffers to access a common hardware page walker

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 3. Document ID: US 6353867 B1

L6: Entry 3 of 12 File: USPT Mar 5, 2002

US-PAT-NO: 6353867
DOCUMENT-IDENTIFIER: US 6353867 B1

h e b b g e e e f e c f ef b e

TITLE: Virtual component on-chip interface

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 4. Document ID: US 6272619 B1

L6: Entry 4 of 12 File: USPT Aug 7, 2001

US-PAT-NO: 6272619
DOCUMENT-IDENTIFIER: US 6272619 B1

TITLE: High-performance, superscalar-based computer system with out-of-order instruction execution

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 5. Document ID: US 6044225 A

L6: Entry 5 of 12 File: USPT Mar 28, 2000

US-PAT-NO: 6044225
DOCUMENT-IDENTIFIER: US 6044225 A

TITLE: Multiple parallel digital data stream channel controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 6. Document ID: US 5822553 A

L6: Entry 6 of 12 File: USPT Oct 13, 1998

US-PAT-NO: 5822553
DOCUMENT-IDENTIFIER: US 5822553 A

TITLE: Multiple parallel digital data stream channel controller architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 7. Document ID: US 5784649 A

L6: Entry 7 of 12 File: USPT Jul 21, 1998

US-PAT-NO: 5784649
DOCUMENT-IDENTIFIER: US 5784649 A

TITLE: Multi-threaded FIFO pool buffer and bus transfer control system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e c f ef b e

☐ 8. Document ID: US 5732094 A

L6: Entry 8 of 12 File: USPT Mar 24, 1998

US-PAT-NO: 5732094
DOCUMENT-IDENTIFIER: US 5732094 A

TITLE: Method for automatic initiation of data transmission

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 9. Document ID: US 5455915 A

L6: Entry 9 of 12 File: USPT Oct 3, 1995

US-PAT-NO: 5455915
DOCUMENT-IDENTIFIER: US 5455915 A

TITLE: Computer system with bridge circuitry having input/output multiplexers and third direct unidirectional path for data transfer between buses operating at different rates

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 5434872 A

L6: Entry 10 of 12 File: USPT Jul 18, 1995

US-PAT-NO: 5434872
DOCUMENT-IDENTIFIER: US 5434872 A

TITLE: Apparatus for automatic initiation of data transmission

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Terms	Documents
L4 and buffer and multiplexer	12

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☐ 11. Document ID: US 5392406 A

Using default format because multiple data bases are involved.

L6: Entry 11 of 12 File: USPT Feb 21, 1995

US-PAT-NO: 5392406
DOCUMENT-IDENTIFIER: US 5392406 A

TITLE: DMA data path aligner and network adaptor utilizing same

DATE-ISSUED: February 21, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Petersen; Brian	Los Altos	CA		
Lo; Lai-Chin	Campbell	CA		
Brown; David R.	San Jose	CA		

US-CL-CURRENT: 710/316; 710/26, 710/3, 712/300

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 12. Document ID: US 5299313 A

L6: Entry 12 of 12 File: USPT Mar 29, 1994

US-PAT-NO: 5299313
DOCUMENT-IDENTIFIER: US 5299313 A

TITLE: Network interface with host independent buffer management

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Terms	Documents
L4 and buffer and multiplexer	12

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US006813673B2

(12) **United States Patent**
Kotlowski et al.

(10) **Patent No.: US 6,813,673 B2**
(45) **Date of Patent: Nov. 2, 2004**

(54) **BUS ARBITRATOR SUPPORTING MULTIPLE ISOCHRONOUS STREAMS IN A SPLIT TRANSACTIONAL UNIDIRECTIONAL BUS ARCHITECTURE AND METHOD OF OPERATION**

(75) Inventors: **Kenneth James Kotlowski**, Berthoud, CO (US); **Brett A. Tischler**, Longmont, CO (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 421 days.

(21) Appl. No.: **09/845,455**

(22) Filed: **Apr. 30, 2001**

(65) **Prior Publication Data**

US 2002/0161953 A1 Oct. 31, 2002

(51) **Int. Cl.**[7] **G06F 13/14; G06F 13/36**
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(56) **References Cited**

U.S. PATENT DOCUMENTS

4,429,405	A	1/1984	Bux et al.	
4,965,828	A	10/1990	Ergott, Jr. et al.	
4,969,120	A *	11/1990	Azevedo et al.	710/117
5,007,011	A	4/1991	Murayama	
5,128,666	A	7/1992	Munier et al.	
5,248,906	A	9/1993	Mahmood	
5,412,786	A	5/1995	Knaack	
5,528,172	A	6/1996	Sundstrom	
5,539,739	A *	7/1996	Dike et al.	370/352
5,577,102	A	11/1996	Koivunen	
5,581,729	A *	12/1996	Nishtala et al.	711/143
5,623,644	A *	4/1997	Self et al.	713/503
5,634,043	A *	5/1997	Self et al.	713/503
5,659,784	A	8/1997	Inaba et al.	
5,694,586	A	12/1997	Eneboe	
5,717,343	A	2/1998	Kwong	

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

DE	19949144	C1	2/2001
JP	10285011	A	10/1998

OTHER PUBLICATIONS

Calder, B. and Grunwald, D., "Fast and Accurate Instruction Fetch and Branch Prediction," Proceedings the 2nd Annual International Symposium on Computer Architecture, Chicago, IL, on pp. 2–11. [online] Retrieved from IEEE Xplore, Abstract, 1 page, Apr. 18, 1994.

(List continued on next page.)

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(57) **ABSTRACT**

In a method and system for transferring data between a plurality of bus devices, a bus interface unit includes a first bus device interface (FBDI), a second bus device interface (SBDI), and an arbitration circuit. Each of the FBDI and SBDI includes a corresponding incoming and outgoing request bus for receiving and transmitting request packets from a corresponding one of the plurality of bus devices. Similarly, each of the EBDI and SBDI also includes a corresponding incoming and outgoing data bus for receiving and transmitting data packets from the corresponding one of the plurality of bus devices. The arbitration circuit is capable of determining priority level associated with corresponding request packets received from the FBDI and the SBDI respectively.

17 Claims, 3 Drawing Sheets